Synchronization of Hardware Simulation Processes

Abstract

A system, method, and computer program product is presented for simulating a system of hardware components. Each component is simulated in a hardware definition language such as VERILOG. Each component is represented as a simulated device under test (DUT) that is incorporated into a simulation module. The invention synchronizes the simulation modules by issuing clock credit to each simulation module. Each simulation module can only operate when clock credit is available, and can only operate for some number of clock cycles corresponding to the value of the clock credit. Operation is said to consume the clock credit. After a simulation module has consumed its clock credit, its DUT halts. Once every simulation module has consumed its clock credit and halted, another clock credit can be issued. This allows checkpointing of the operation of each DUT and simulates parallelism of the DUTs using executable images of manageable size. A given DUT can include two or more subsets of logic that each require a clock signal having a different rate. Such subsets of the logic of a DUT are referred to as clock domains. The appropriate clock signals are created by a test bench component of the simulation module. The test bench creates a master clock signal for the DUT. The test bench then divides this clock signal to produce clock signals applied to the clock domains of the DUT. The test bench can be created through automated means by providing a system specification that defines the inputs (including clocks) and outputs of a DUT. This allows a test bench specific to the DUT to be created.